

Preliminary SCT2168S V00_01; Mar/11

8-bit Serial-In/Parallel-Out Constant Current Driver

Product Description

The SCT2168S serial-interfaced LED driver sinks 8 LED clusters with constant current to keep the uniform intensity of LED displays. In applications, an external resistor is used to set the full-scale constant output current from 10mA up to 90mA. The SCT2168S guarantees each output can endure maximum 17V DC voltage stress. The built-in shift registers and data latches making the SCT2168S effective solution in driving LED display. The output enable function gates all 8 outputs on and off, and is fast enough to be used as PWM input for LED intensity control. Since the serial data input rate can be reached up to 25MHz, the SCT2168S will satisfy system which needs high volume data transmission to control the LED

Features

- 8 constant current sinkers with output voltage sustainable to 17V
- Constant output current : 10 60/90mA@3.3/5V
- Excellent regulation to load, supply voltage and temperature
 Temperature regulation: ±0.005%/°C, load regulation: ±0.1%/V, line regulation: ±0.5%/V
- High current matching accuracy: ±1% between outputs, ±2% between ICs
- Fast output current control: Minimum PWM pulse width = 200ns
- Low dropout voltage 0.5V@40mA, V_{DD}=5V
- All output current are programmed together using a single external resistor
- CMOS Schmitt trigger inputs with clock rate up to 25MHz
- Operating supply voltage range of 3.3V to 5.5V
- Built-in power on reset circuit forces all the outputs off while power on
- Package: SSOP16
- Applications: LED Displays, Variable Message Signs, LED Traffic Signs

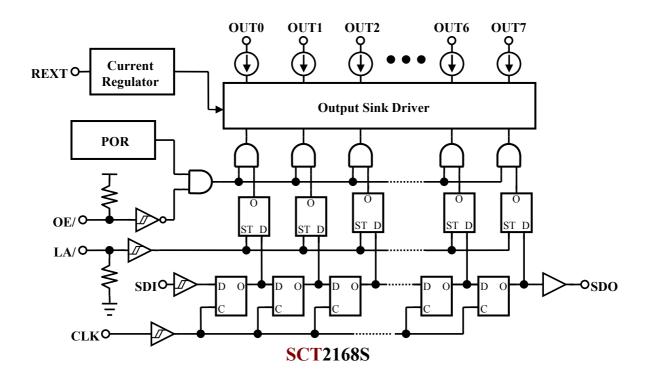
Pin Configurations

GND SDI CLK LA/ OUT0 OUT1 OUT2 OUT3	1 ● 2 3 4 5 6 7 8	SCT2168S SSSG	16 15 14 13 12 11 10 9	 □ VDD □ REXT □ SDO □ OE/ □ OUT7 □ OUT6 □ OUT5 □ OUT4
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Terminal Description

Pin Name	Pin No.	I/O	Function
GND	1	-	Ground terminal
SDI	2	Ι	Serial input terminal of data shift register
CLK	3	I	Clock input terminal of shift register, data is sampled at the rising edge of CLK.
LA/	4	I	Data is latched when LA/ is low. Data on shift register goes through when LA/ is high.
OUT[0:7]	5-12	0	Open-drain, constant-current outputs.
OE/	13	I	Input terminal of output enable signal. Output is enabled when OE/ is low.
SDO	14	0	Output terminal of serial-data output to the SDI of next SCT2168S.
REXT	15	I/O	Synchronous signal, daisy chain output terminal.
VDD	16	-	Supply voltage terminal

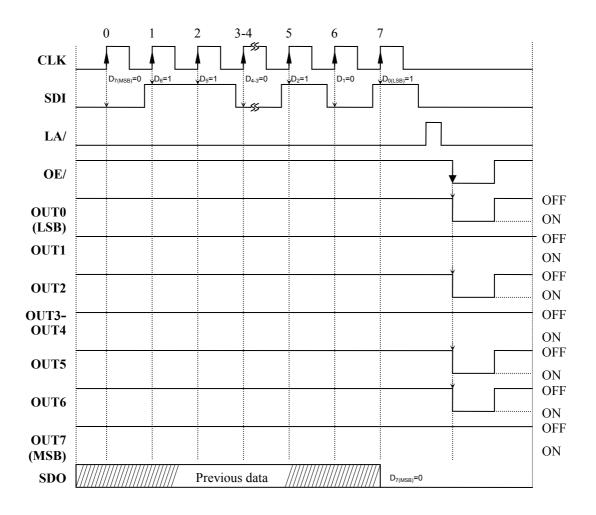
Block Diagram



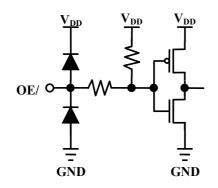
CLK	LA/	OE/	SDI	OUT0 ~ OUT7	SDO
_	Н	L	D _n	D _n D _{n-1} D _{n-6} D _{n-7}	D _{n-7}
_	L	L	D _{n+1}	No change	D _{n-6}
	Н	L	D _{n+2}	D _{n+2} D _{n+1} D _{n-4} D _{n-5}	D _{n-5}
▼	Х	L	D _{n+3}	D _{n+2} D _{n+1} D _{n-4} D _{n-5}	D _{n-5}
	Х	Н	D _{n+3}	Off	D _{n-5}

Truth Table

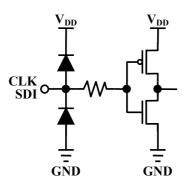
Timing Diagram



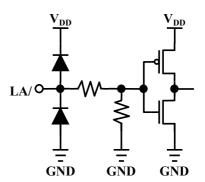
Equivalent Circuits of Inputs (1)



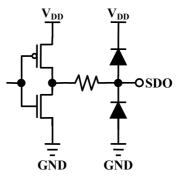
Equivalent Circuits of Inputs (3)



Equivalent Circuits of Input (2)



Equivalent Circuits of Output



Selector Guide

Part	Number of Outputs	Max Output Current (mA)	Min PWM Pulse Width (ns)	Supply Voltage (V)	Error Detection
SCT2110	8	180	100	5	NA
SCT2168	8	120	120	3.3/5	NA
SCT2169	8	120	120	3.3/5	Yes
SCT2167	8	60	180	3.3/5	NA
SCT2210	16	120	50	5	NA
SCT2026	16	90	120	3.3/5	NA
SCT2027	16	90	120	3.3/5	Yes
SCT2024	16	60	180	3.3/5	NA

Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT2168SSSG	SCT2168SSSG	Green SSOP16	2500

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Maximum Ratings (T_A = 25°C)

Charact	eristic	Symbol	Rating	Unit
Supply voltage		V _{DD}	7.0	V
Input voltage		V _{IN}	$-0.2 \sim V_{DD} + 0.2$	V
Output current		I _{OUT}	100	mA/Channel
Output voltage	Outputs	- V _{out}	$-0.2 \sim V_{DD} + 0.2$	V
Oulput vollage	OUT0~OUT7	VOUT	-0.2 ~ 17	V
Total GND terminals cu	rrent	I _{GND}	800	mA
Power dissipation	SSOP16	PD	1.07	W
Thermal resistance	SSOP16	R _{TH(j-a)}	117	°C /W
Operating junction temperature		T _{J(max)}	150	С°
Operating temperature		T _{OPR}	-40~+85	°C
Storage temperature		T _{STG}	-55~+150	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_A= -40 to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Тур.	Max.	Unit
Supply voltage	V _{DD}	-	3	-	5.5	V
Output voltage	V	Output OFF	-	-	17	V
Output voltage	V _{OUT}	Output ON	-	1 ¹	4 ²	V
Output current	I _{OUT}	V _{DD} =3.3/5V, V _{OUT} =1V	10	-	60/90	mA
Input voltage	V _{IH}	input signals	0.7V _{DD}	-	V _{DD}	V
input voltage	V _{IL}	input signals	0	-	$0.3V_{DD}$	V
OE/ pulse width	t _{W(OE)}	V _{DD} =3.3V/5V	200	-	-	ns

1. The output current keep constant in range of 10-90mA if $V_{\mbox{\scriptsize OUT}}\mbox{=}1V.$

However, user can minimize V_{OUT} to reduce power dissipation according to used current, e.g., set V_{OUT} to 0.5V if I_{OUT}=20mA.
 The maximum Vout is package thermal limited, user should keep Vout under maximum power dissipation.

Characteristic		Symbol	Conditions	Min.	Тур.	Max.	Unit
Disital inputs valtage		V _{IH}	-	0.7V _{DD}	-	V _{DD}	V
Digital inputs volt	aye	V _{IL}	-	0	-	$0.3V_{\text{DD}}$	V
SDO output volta	00	V _{OH}	V _{DD} =3.3/5V, I _{OH} = -1mA	V _{DD} -0.4	-	-	V
	ge	V _{OL}	V _{DD} =3.3/5V, I _{OL} = +1mA	-	-	0.4	V
Output leakage c	urrent	I _{OL}	V _{OUT} =17V	-	-	0.5	uA
Output current		I _{OUT}	V_{OUT} =1V, R_{EXT} =900 Ω	-	42	-	mA
Current bit skew ¹		dl _{OUT1}	V_{OUT} =1V, R _{EXT} =900 Ω	-	±1	±2	%
Chip skew ²		dl _{OUT2}	V_{OUT} =1V, R_{EXT} =900 Ω	-	±2	±4	%
Line regulation ³ I_{OUT} vs. V_{DD}		%/dV _{DD}	3V <v<sub>DD<5.5V, V_{OUT}>1V, R_{EXT}=900Ω</v<sub>	-	±0.5	±1	%/V
Load regulation ⁴ I _{OUT} vs. V _{OUT}		%/dV _{OUT}	1V <v<sub>OUT<4V, I_{OUT}=42mA, R_{EXT}=900Ω</v<sub>	-	±0.1	±0.5	%/V
Temp. regulation ⁵ I _{OUT} vs. T _A		%/dT _A	-20°C < T _A < 80°C, I _{OUT} =10mA~90mA,V _{DD} =5V	-	±0.005	-	%/°C
Pull-up resistor		R _{UP}	OE/	-	420	-	KΩ
Pull-down resisto	r	R _{DOWN}	LA/	-	400	-	KΩ
	I _{DD(OI}	I _{DD(OFF)1}	V _{DD} =3.3/5V, R _{EXT} =Open, OUT[0:7]=OFF	-	2	3	
Supply current	OFF	I _{DD(OFF)2}	V _{DD} =3.3/5V, R _{EXT} =900Ω, OUT[0:7]=OFF	-	5	7	mA
	ON	I _{DD(ON)}	V_{DD} =3.3/5V, R _{EXT} =900 Ω , OUT[0:7]=ON	-	7/8	10	

Electrical Characteristics (V_{DD}=3.3/5V, T_A=25°C unless otherwise noted)

1. Bit skew=(I_{OUT} - I_{AVG}) / I_{AVG} , where I_{AVG} =($I_{OUT(max)}$ + $I_{OUT(min)}$)/2

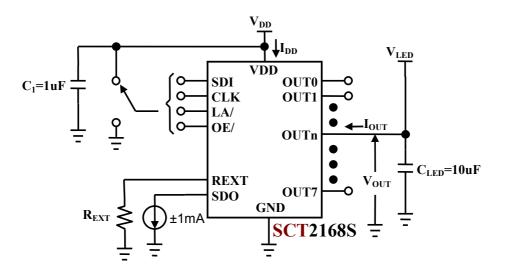
2. Chip skew=(I_{AVG} - I_{CEN}) / I_{CEN} *100(%), where I_{CEN} is the statistics distribution center of output currents.

3. Line regulation=[$I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)$] / {[$I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)$]/2} / (5.5V-3V)*100(%/V)

4. Load regulation=[$I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)$] / {[$I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)$]/2} / (4V-1V)*100(%/V)

5. Temperature regulation=[$I_{OUT}(T_A=80^{\circ}C)-I_{OUT}(T_A=-20^{\circ}C)$] / {[$I_{OUT}(T_A=80^{\circ}C)+I_{OUT}(T_A=-20^{\circ}C)$]/2} / (80^{\circ}C+20^{\circ}C)*100(%/^{\circ}C)

Test Circuit for Electrical Characteristics



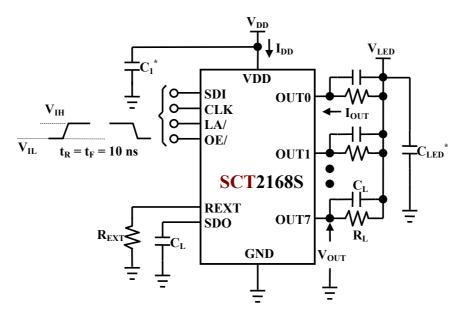
*Place C₁/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.

Characte	ristic	Symbol	Conditions	Min.	Тур.	Max.	Unit
	CLK - OUTn	t _{PLH1}		-	80	100	ns
Propagation delay	LA/ - OUTn	t _{PLH2}		-	80	100	ns
time ("L" to "H")	OE/ - OUT0	t _{PLH3}		-	80	100	ns
	CLK - SDO	t _{PLH}		-	20	40	ns
	CLK - OUTn	t _{PHL1}		-	80	100	ns
Propagation delay	LA/ - OUTn	t _{PHL2}		-	80	100	ns
time ("H" to "L")	OE/ - OUT0	t _{PHL3}	$V_{DD} = 3.3/5V$	-	80	100	ns
	CLK - SDO	t _{PHL}	$V_{LED} = 5V$ $V_{IH} = V_{DD}$	-	20	40	ns
	CLK	t _{W(CLK)}	V _{IL} = GND	20	-	-	ns
Pulse width	LA/	t _{W(L)}	$R_{EXT} = 900\Omega$ $R_{L} = 90\Omega$ $C_{L} = 10pF$ $C_{1} = 1uF$ $C_{LED} = 100uF$	20	-	-	ns
	OE/	t _{W(OE)}		180	-	-	ns
Setup time for SDI		t _{S(D)}		5	-	-	ns
Hold time for SDI		t _{HD)}		15			ns
Setup time for LA/		t _{S(L)}		5	-	-	ns
Hold time for LA/		t _{H(L)}		5	-	-	ns
SDO rise time		t _{sdor}		-	20	-	ns
SDO fall time		t _{SDOF}		-	20	-	ns
Output rise time of I _{OUT}		t _{OR}		-	80	100	ns
Output fall time of I _{OUT}		t _{OF}		-	80	100	ns
Slow CLK rise time ¹	Slow CLK rise time ¹		Cascade	-	-	500	ns
Slow CLK fall time		t _F	Cascaue	-	-	500	ns

Switching Characteristics (T_A=25°C unless otherwise noted)

1. It may not be possible to achieve the timing required for data transfer between two cascaded drivers if t_R/t_F is large.

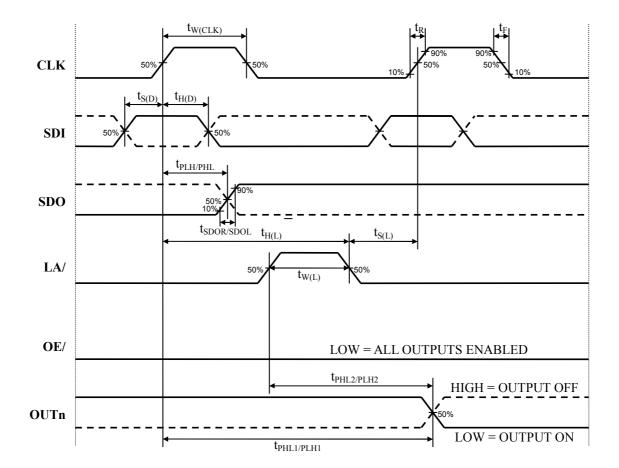
Test Circuit for Switching Characteristics



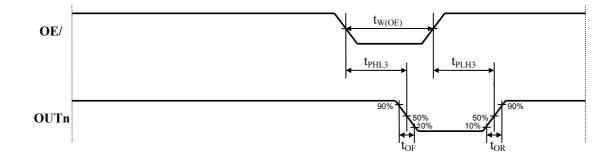
*Place C_1/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.

Timing Waveform

LA/ Control Output

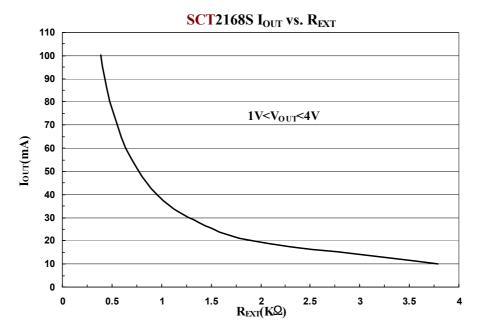


OE/ Control Output



Adjusting Output Current

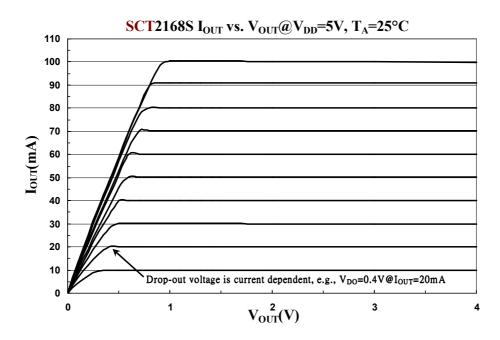
The SCT2168S's output current (I_{OUT}) are set by one external resistor at pin REXT. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

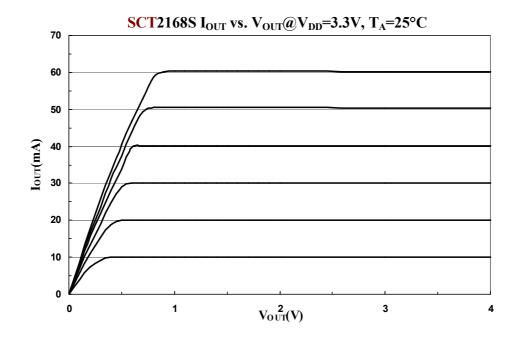


According to SCT2168S' I-V curve, the output voltage should be larger than 1V to get 100 mA constant current. By applying proper output voltage, the SCT2168S' output current set by an external resistor is approximate to: $I_{OUT} = 60(630 / \text{REXT})$ (mA) (chip skew < ±4%). Thus the output current is set to be about 42mA at REXT = 900 Ω .

Output Characteristics

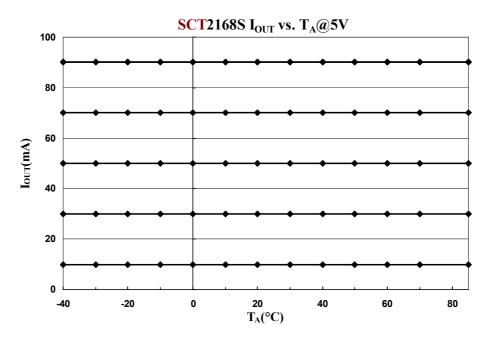
The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when $V_{OUT} > V_{DO}$. The relationship between I_{OUT} and V_{OUT} is shown below. The output voltage should be kept as low as possible to prevent the SCT2168S from being overheated.





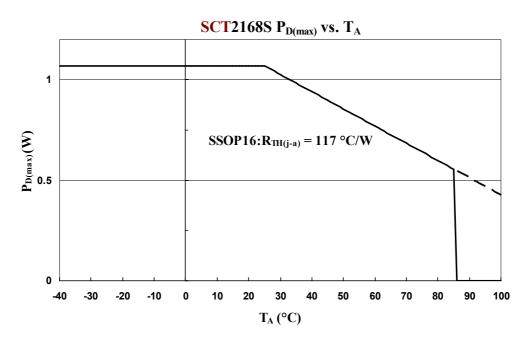
Excellent Temperature Regulation

The constant current driver requires not only the characteristics of supply and load voltage independence, but also temperature invariance. A well thermal stable reference circuit is designed within the SCT2168S. Users can get the stable output current over recommended current range I_{OUT} =10mA~90mA with ambient temperature (T_A) widely varying from -40°C to 85°C.



Power Dissipation

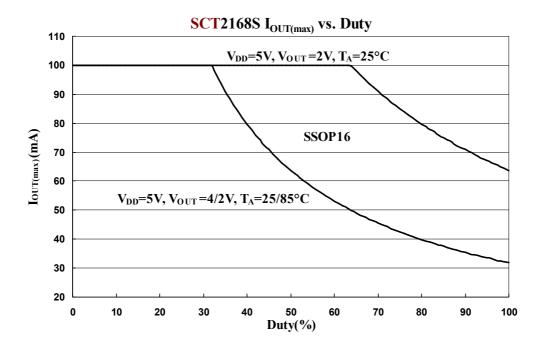
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)}-T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A : ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sinking larger I_{OUT} , users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT2168S.



Limitation on Maximum Output Current

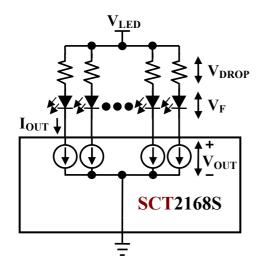
The maximum output current vs. duty cycle is estimated by:

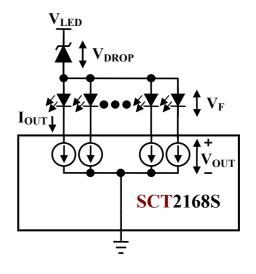
 $I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(V_{DD}*I_{DD}))/V_{OUT}/Duty/N \text{ where } T_{J(max)}=150^{\circ}\text{C}, \text{ N=8(all ON)}$



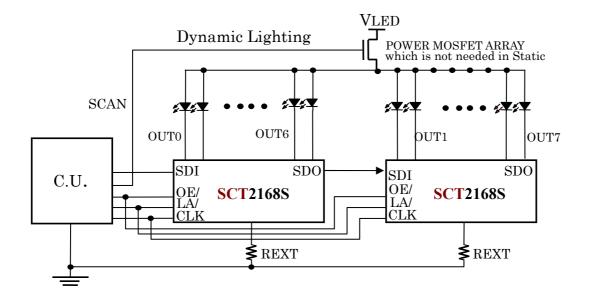
Load Supply Voltage (VLED)

The SCT2168S can be operated very well when V_{OUT} ranges from 1V to 4V. However, it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT2168S. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.





Typical Application

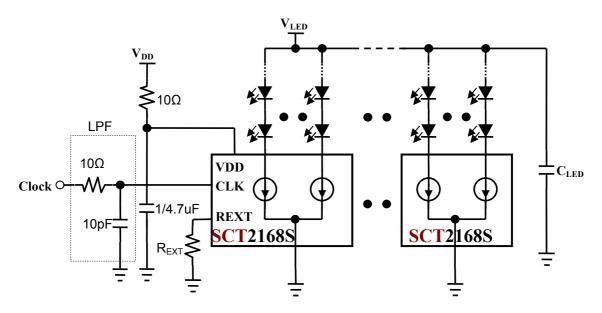


PCB Design Considerations

Use the following general guide-line when designing printed circuit boards (PCB):

Decoupling Capacitor

Place a decoupling capacitor, e.g., 1uF between VDD and GND pins of SCT2168S. Locate the capacitor as close to the SCT2168S as possible. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



External Resistor (R_{EXT})

Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

Power and Ground

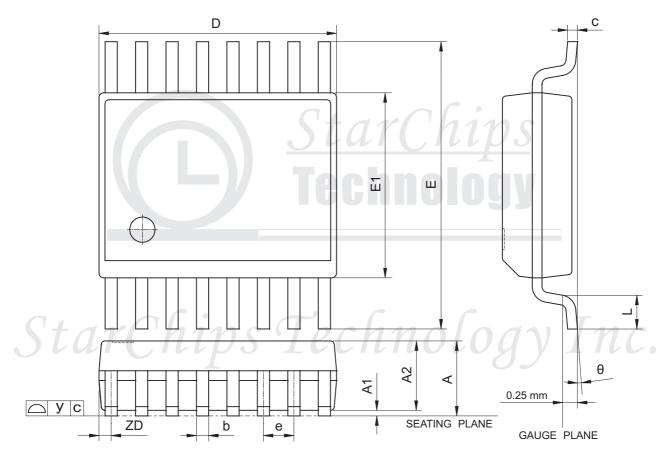
Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if I_{OUT} is larger) series in power input of the SCT2168S in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V_{LED} , furthermore adding a capacitor C_{LED} greater than 10uF beside the LED are recommended. Please adapt C_{LED} according to total system current consumption.

EMI Reduction

To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

Package Dimension

SSOP16(check up-to-date version)



Symbol	D	imension (mr	n)	D	imension (mi	l)
Symbol	Min.	Nom.	Max.	Min.	Nom.	Max.
А	1.35	1.63	1.75	53.1	64.2	68.9
A1	0.10	0.15	0.25	3.9	5.9	9.8
A2	-	-	1.50	-	-	59.1
b	0.20	-	0.30	7.9	-	11.8
С	0.18	-	0.25	7.1	-	9.8
D	4.80	4.90	5.00	189.0	192.9	196.9
E	5.79	5.99	6.20	228.0	235.8	244.1
E1	3.81	3.91	3.99	150.0	153.9	157.1
е		0.64 BSC			25.0 BSC	
L	0.41	0.64	1.27	16.1	25.0	50.0
у	-	-	0.10	-	-	3.9
ZD	0.23 REF				9.0 REF	
θ	0°	-	8°	0°	-	8°

Revision History(check up-to-date version)

Data Sheet Version	Remark
V00_01	Preliminary Release

Information provided by StarChips Technology is believed to be accurate and reliable. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Starchips can not assume responsibility and any problem raising out of the use of the circuits. Starchips reserves the right to change product specification without prior notice.

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