16-bit Serial-In/Parallel-Out Constant-Current LED Driver

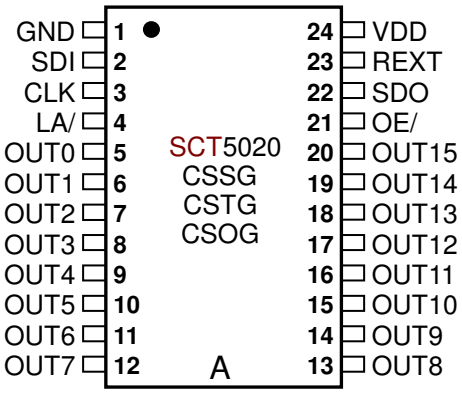
Product Description

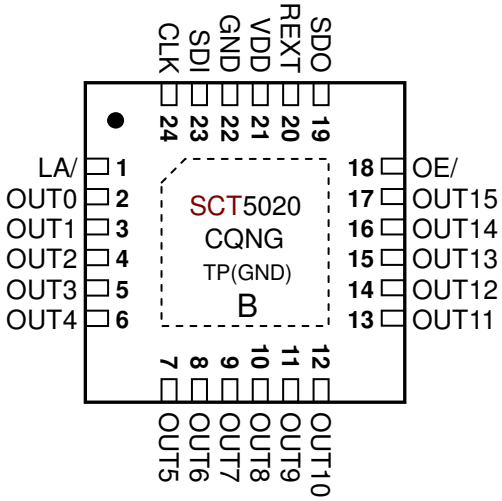
The SCT5020 provides 16 LED constant current sinkers to drive LED displays with uniform intensity. In applications, an external resistor is used to set the full-scale constant output current from 1mA up to 90mA. The SCT5020 ensures that each output can endure maximum 17V DC voltage stress. The shift registers and data latches make the SCT5020 an effective solution for driving LED display. The output enable function gates the on and off of all 16 outputs and is fast enough to be used as a PWM input for LED intensity control. With a serial data rate of up to 25MHz, the SCT5020 meets the needs of LED displays that require large amounts of data.

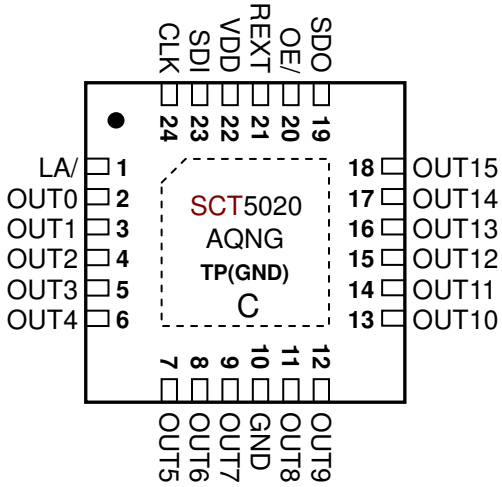
Features

- Current accuracy : ±1% between outputs, ±2% between Ics
- ESD protection ability : HBM > 8KV, MM > 350V
- Finest PWM pulse width : 40nS
- Output withstand voltage : 17V
- Constant output current range : 1~60mA @V_{OUT}=1V, V_{DD}=5V
- Power supply voltages: 3.3V to 5V
- Excellent current regulation : Load regulation: ±0.1%/V, Line regulation: ±0.5%/V
- Low dropout voltage 0.5V@20mA, V_{DD}=5V
- CMOS Schmitt trigger inputs with clock rate up to 25MHz
- The output current is set by an external resistor
- All outputs are turned off while power on
- Package: SSOP24, SSOP24-1, SOP24 and TQFN24
- Applications: LED Displays, Variable Message Signs, LED Traffic Signs and indicators

Pin Configurations



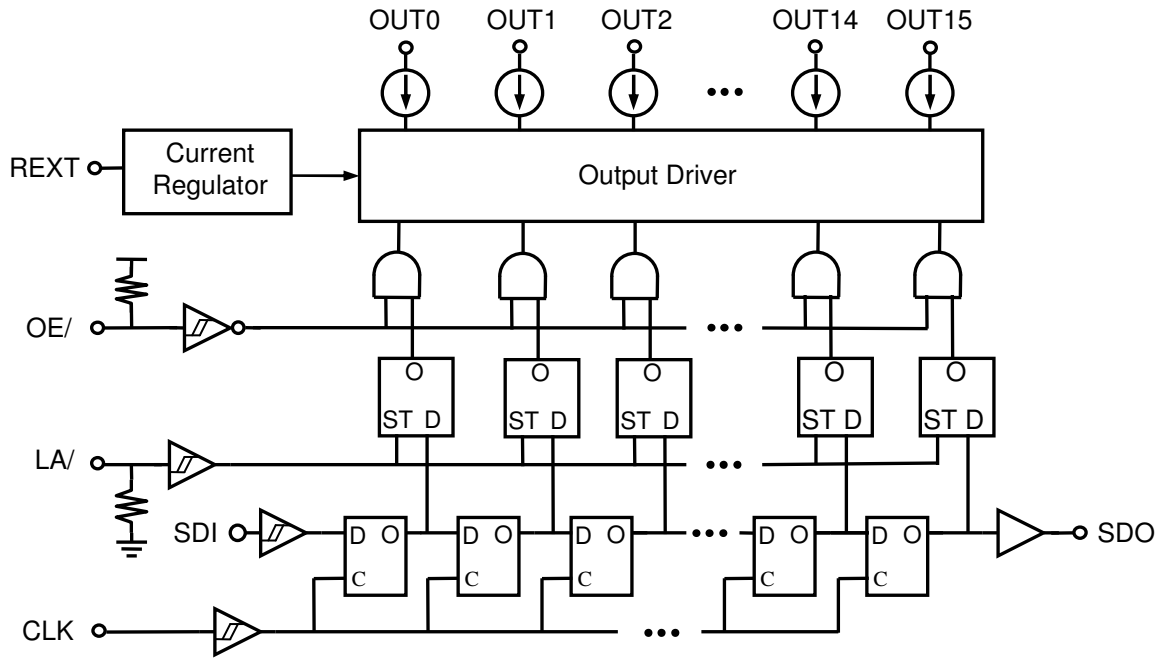




Terminal Description

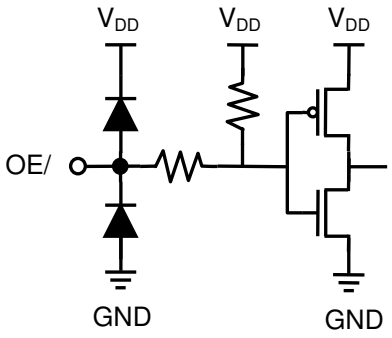
Pin Name	Pin No.			I/O	Function
	A	B	C		
GND	1	22 (TP)	10 (TP)	-	Ground terminal(TP, thermal pad included)
SDI	2	23	23	I	Serial data input pin.
CLK	3	24	24	I	Clock input pin, data is sampled at the rising edge of CLK.
LA/	4	1	1	I	Data strobe input. Data is latched when LA/ is low. And data goes through when LA/ is high.
OUT[0:15]	5-20	2-17	2-9 11-18	O	Open-drain, constant-current outputs.
OE/	21	18	20	I	Output enable signal. Output is enabled when OE/ is forced to low.
SDO	22	19	19	O	Serial-data output pin which is connected to the SDI of next SCT5020.
REXT	23	20	21	I/O	Connect this pin to an external resistor for setting all output current
VDD	24	21	22	-	Supply voltage terminal

Block Diagram

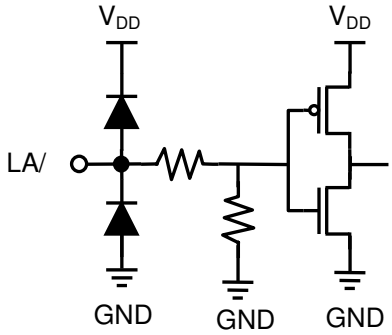


SCT5020

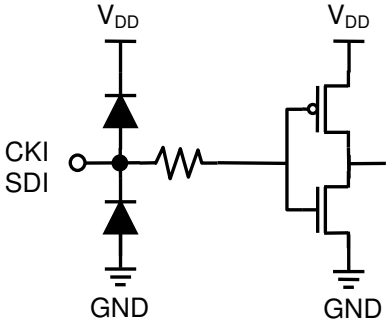
Equivalent Circuits of Inputs (1)



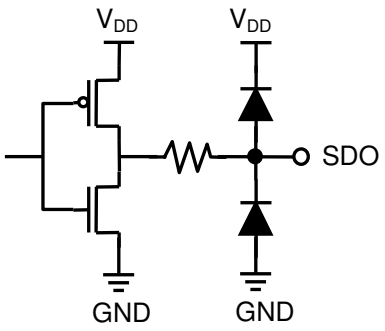
Equivalent Circuits of Inputs (2)



Equivalent Circuits of Inputs (3)



Equivalent Circuits of Output



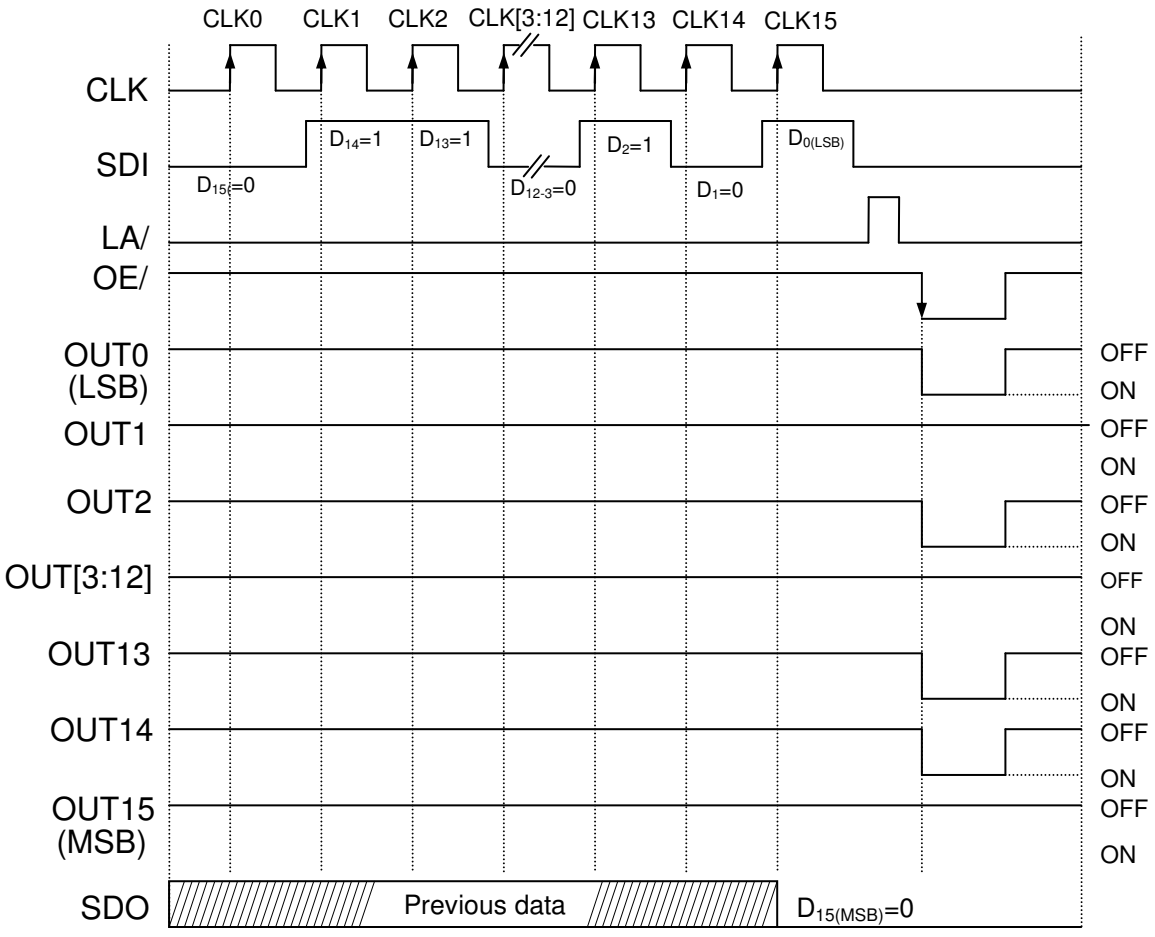
Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT5020CSSG	SCT5020CSSG	Green SSOP24	2500
SCT5020CSTG	SCT5020CSTG	Green SSOP24-1	2000
SCT5020CSOG	SCT5020CSOG	Green SOP24	1000
SCT5020CQNG	5020CQNG	Green TQFN24	3000
SCT5020AQNG	5020AQNG	Green TQFN24	3000

Truth Table

CLK	LA/	OE/	SDI	OUT0 ~ OUT15	SDO
↑	H	L	D_n	D_n D_{n-1} ---- D_{n-14} D_{n-15}	D_{n-15}
↑	L	L	D_{n+1}	No change	D_{n-14}
↑	H	L	D_{n+2}	D_{n+2} D_{n+1} ---- D_{n-12} D_{n-13}	D_{n-13}
↓	X	L	D_{n+3}	D_{n+2} D_{n+1} ---- D_{n-12} D_{n-13}	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Timing Diagram



Maximum Ratings (T_A = 25℃)

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{DD}	7.0	V
Input voltage		V_{IN}	-0.2 to V_{DD}+0.2	V
Output current		I_{OUT}	90 (V_{OUT}>1.9V)	mA/Channel
Output voltage	SDO	V_{OUT}	-0.2 to V_{DD}+0.2	V
	OUT0~OUT15		-0.2 to 17	V
Total GND terminals current		I_{GND}	960	mA
Power dissipation	SOP24	P_D	1.92	W
	SSOP24		1.42	
	SSOP24-1.0		1.74	
	TQFN24		2.08	
Thermal resistance	SOP24	$R_{TH(j-a)}$	65	℃ /W
	SSOP24		88	
	SSOP24-1.0		72	
	TQFN24		60	
Operating junction temperature		$T_{J(max)}$	150	℃
Operating temperature		T_{OPR}	-40 to +85	℃
Storage temperature		T_{STG}	-55 to +150	℃

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration or even permanent damage. Prolonged exposure to maximum rated conditions may affect the reliability of the device.

Recommended Operating Conditions (T_A= -40 to 85℃ unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3	-	5.5	V
Output voltage	V_{OUT}	Output OFF	-	-	17	V
		Output ON	-	1[1]	4[2]	V
Output current	I_{OUT}	V_{DD}=3.3/5V	1	-	40/90	mA
Input voltage	V_{IH}	Input signals	0.7V_{DD}	-	V_{DD}	V
	V_{IL}	Input signals	0	-	0.3V_{DD}	V
OE/ pulse width	$t_{W(OE)}$	V_{DD}=3.3V/5V	40	-	-	nS

1. The output current keeps constant in range of 1-90mA if V_{OUT}>=1V.
However, user can minimize V_{OUT} to reduce power dissipation, e.g., set V_{OUT} to 0.6V if I_{OUT}=20mA.

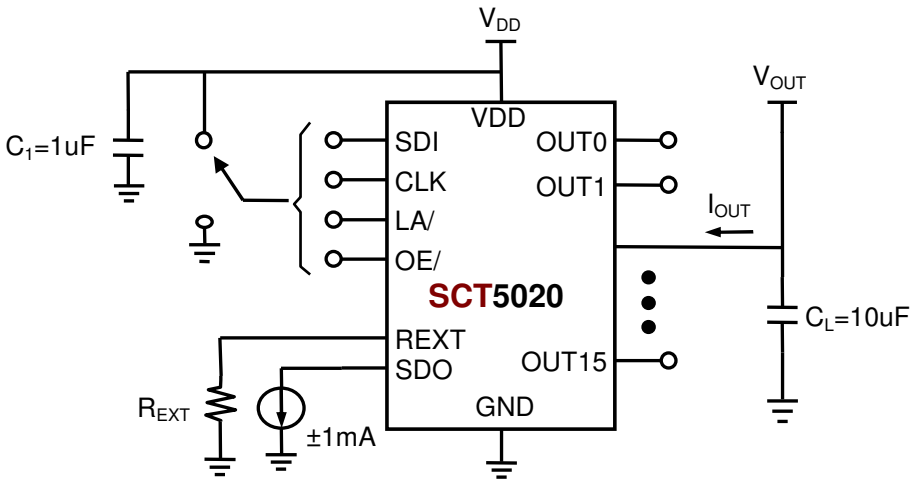
2. The maximum Vout is limited by the package thermal and output duty; user should keep Vout under the maximum power dissipation.

Electrical Characteristics (V_{DD}=3.3/5V, T_A=25℃ unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage		V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
		V_{IL}	-	0	-	0.3V_{DD}	V
SDO output voltage		V_{OH}	V_{DD}=3.3/5V, I_{OH}= -1mA	V_{DD}-0.4	-	-	V
		V_{OL}	V_{DD}=3.3/5V, I_{OL}=+1mA	-	-	0.4	V
Output leakage current		I_{OL}	V_{OUT}=17V	-	-	0.5	uA
Output current		I_{OUT}	V_{OUT}=1V, R_{EXT}=900Ω	-	20.5	-	mA
Current bit skew[1]		dI_{OUT1}	V_{OUT}=1V, R_{EXT}=900Ω	-	±1	±2	%
Chip skew[2]		dI_{OUT2}	V_{OUT}=1V, R_{EXT}=900Ω	-	±2	±3	%
Line regulation[3] I_{OUT} vs. V_{DD}		%/dV_{DD}	3V<V_{DD}<5.5V, V_{OUT}=1V, R_{EXT}=900Ω	-	±0.5	±1	%/V
Load regulation[4] I_{OUT} vs. V_{OUT}		%/dV_{OUT}	1V<V_{OUT}<4V, I_{OUT}=20.5mA, R_{EXT}=900Ω	-	±0.1	±0.5	%/V
Pull-up resistor		R_{UP}	OE/	-	400	-	KΩ
Pull-down resistor		R_{DOWN}	LA/	-	400	-	KΩ
Supply current	OFF	$I_{DD(OFF)1}$	V_{DD}=3.3/5V, R_{EXT}=Open, OUT[0:15]=OFF(=VDD)	-	3	4	mA
	OFF	$I_{DD(OFF)2}$	V_{DD}=3.3/5V, R_{EXT}=900Ω, OUT[0:15]=OFF(=VDD)	-	5	7	mA
	ON	$I_{DD(ON)}$	V_{DD}=3.3/5V, R_{EXT}=900 Ω, OUT[0:15]=ON	-	7/8	10	mA

1. Bit skew=(I_{OUT}-I_{AVG}) / I_{AVG}, where I_{AVG}=($I_{OUT(max)}$+ $I_{OUT(min)}$)/2
*2. Chip skew=(I_{AVG}-I_{CEN}) / I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.*
*3. Line regulation=[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)] / {[I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2} / (5.5V-3V)*100(%/V)*
*4. Load regulation=[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)] / {[I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2} / (4V-1V)*100(%/V)*

Test Circuit for Electrical Characteristics

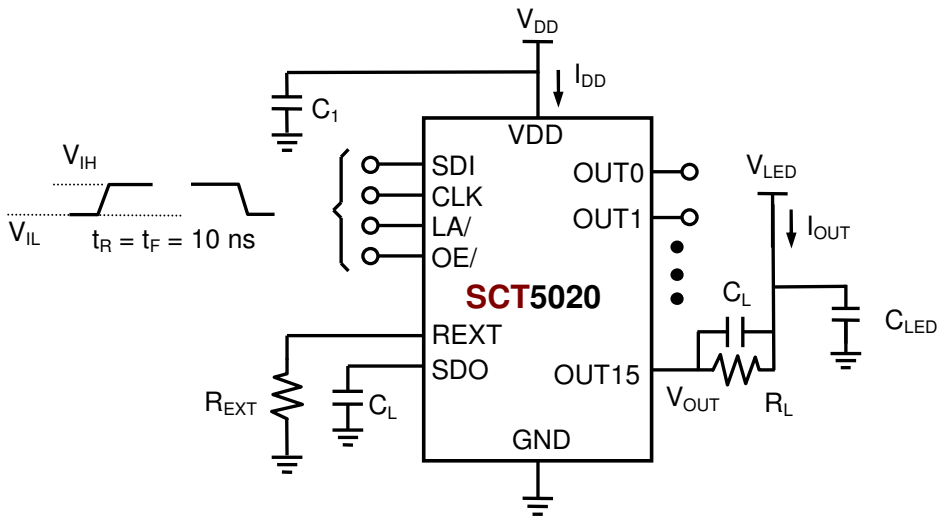


Switching Characteristics (T_A=25℃ unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time (“L” to “H”)	CLK - OUTn	t_{PLH1}	V_{DD} = 3.3/5V V_{LED} = 5V V_{IH} = V_{DD} V_{IL}= GND R_{EXT} = 900Ω R_L = 180Ω C_L = 10pF C_1 = 1uF C_{LED} = 10uF	-	80	150	nS
	LA/ - OUTn	t_{PLH2}		-	80	150	nS
	OE/ - OUT0	t_{PLH3}		-	80	150	nS
	CLK - SDO	t_{PLH}		-	20	40	nS
Propagation delay time (“H” to “L”)	CLK - OUTn	t_{PHL1}		-	80	150	nS
	LA/ - OUTn	t_{PHL2}		-	80	150	nS
	OE/ - OUT0	t_{PHL3}		-	80	150	nS
	CLK - SDO	t_{PHL}		-	20	40	nS
Pulse width	CLK	$t_{W(CLK)}$		20	-	-	nS
	LA/	$t_{W(L)}$		20	-	-	nS
	OE/	$t_{W(OE)}$		25	40	-	nS
Setup time for SDI		$t_{S(D)}$		5	-	-	nS
Hold time for SDI		$t_{HD)}$		15			nS
Setup time for LA/		$t_{S(L)}$		5	-	-	nS
Hold time for LA/		$t_{H(L)}$		5	-	-	nS
SDO rise time		t_{SDOR}		-	10	-	nS
SDO fall time		t_{SDOF}		-	10	-	nS
Output rise time of I_{OUT}		t_{OR}		-	40	60	nS
Output fall time of I_{OUT}		t_{OF}		-	40	60	nS
Slow CLK rise time*		t_R	Cascade	-	-	500	nS
Slow CLK fall time		t_F		-	-	500	nS

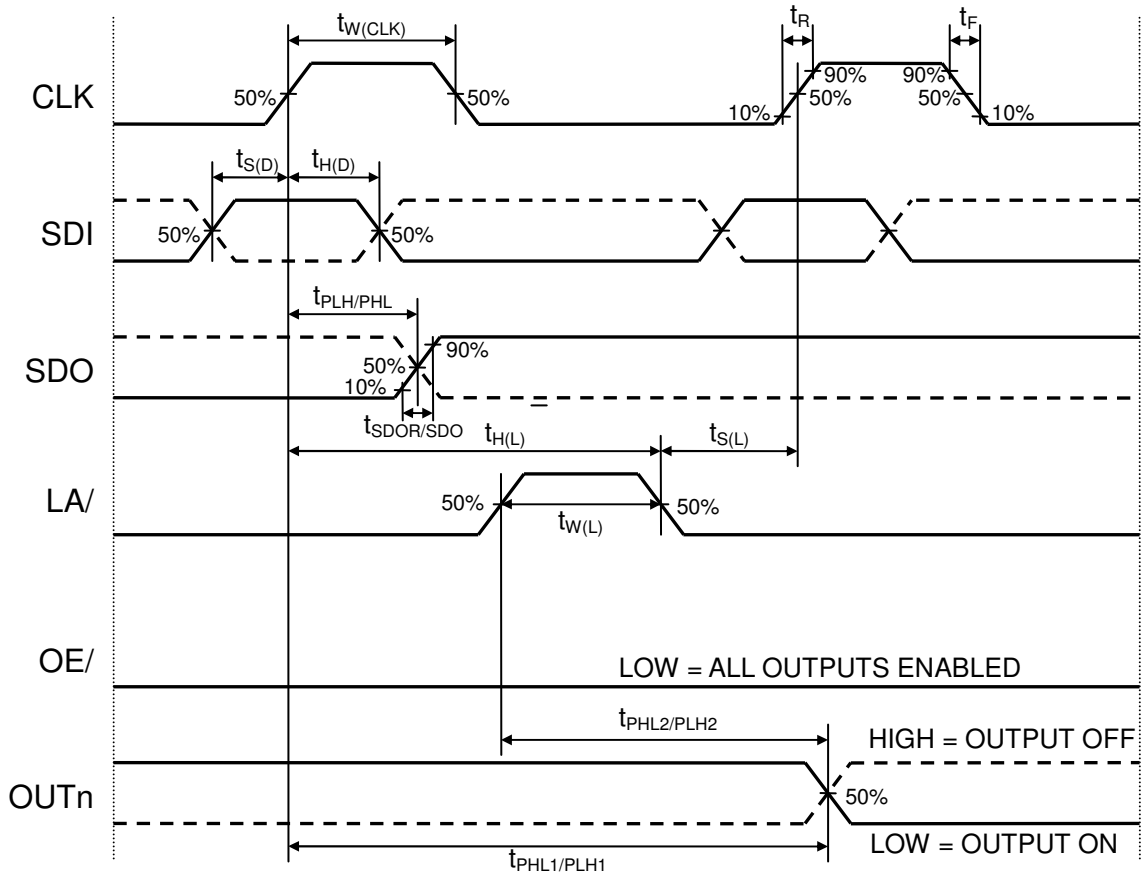
**It may not be possible to achieve the timing requirment for data transfer if t_R and t_F is too large during cascaded operation.*

Test Circuit for Switching Characteristics

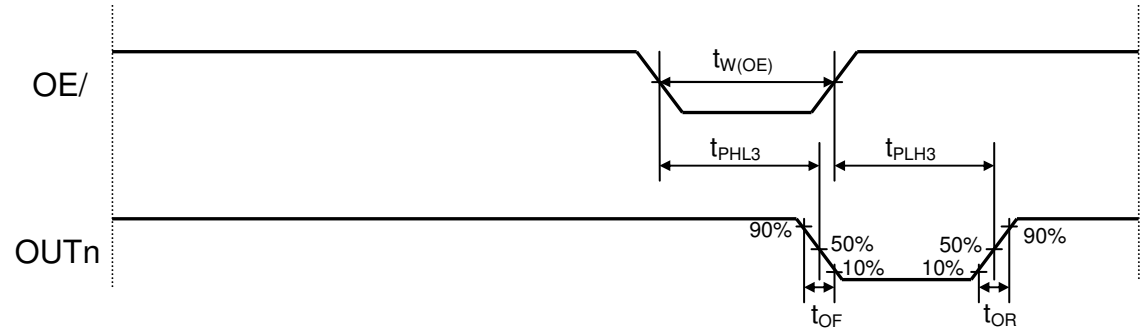


Timing Waveform

LA/ control outputs

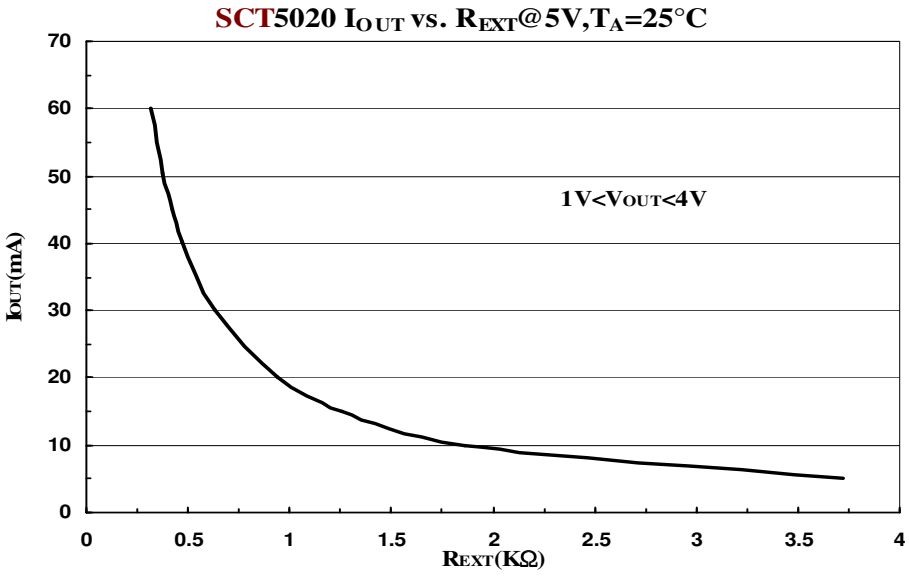


OE/ control outputs



Adjusting Output Current

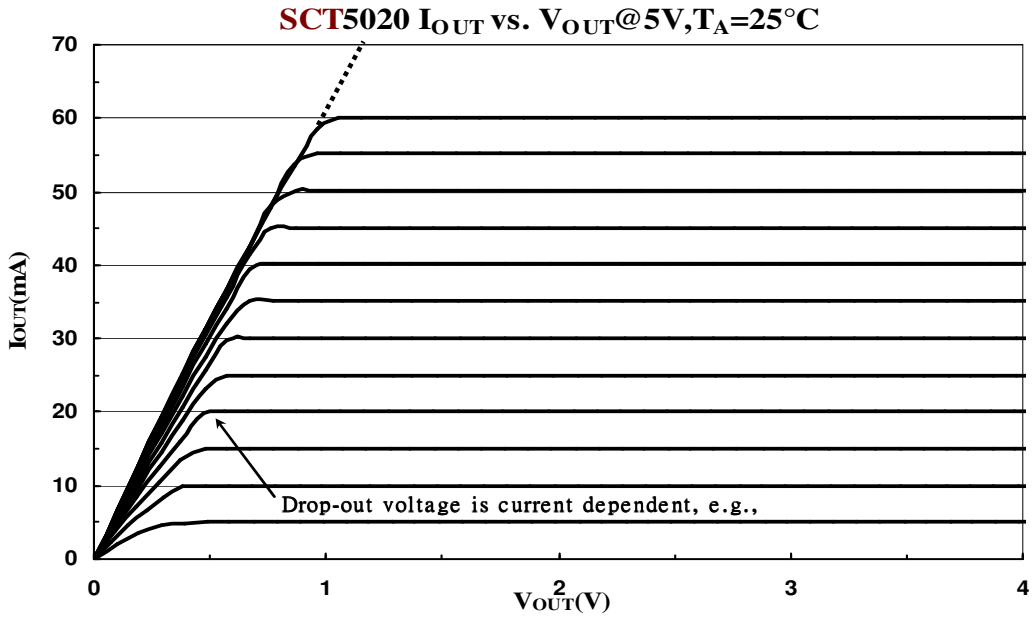
The output current (I_{OUT}) of the SCT5020 is set by an external resistor on the REXT pin. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

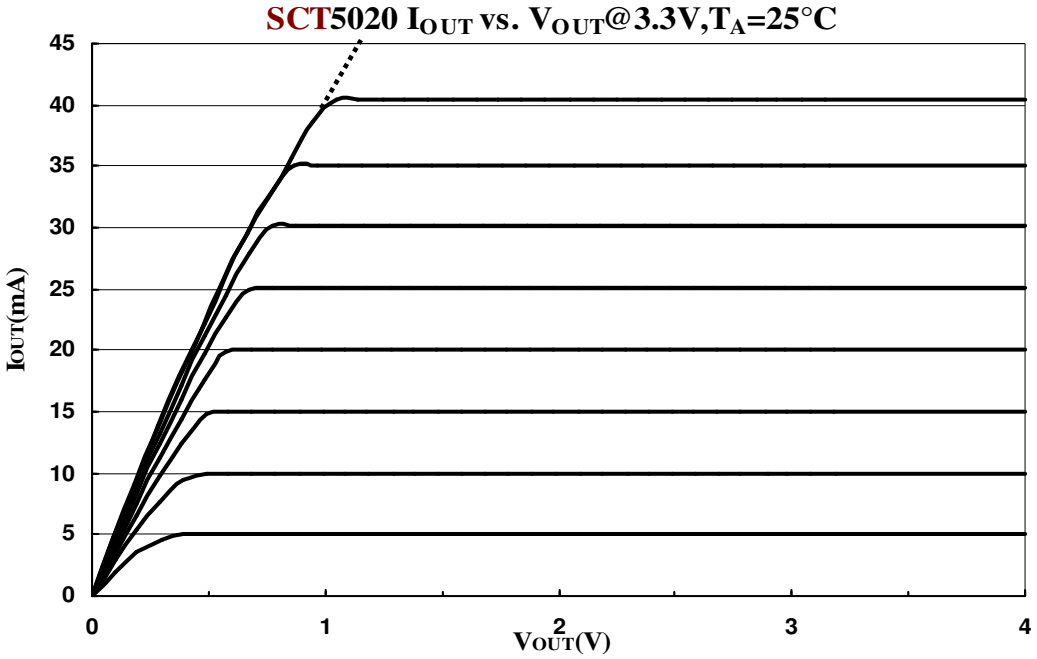


When the output voltage is larger than 1V, the constant output current set by REXT is approximate to I_{OUT} (mA) = 18.45/ REXT (KΩ). Thus the output current is about 20.5mA at REXT = 0.9KΩ.

Output Characteristics

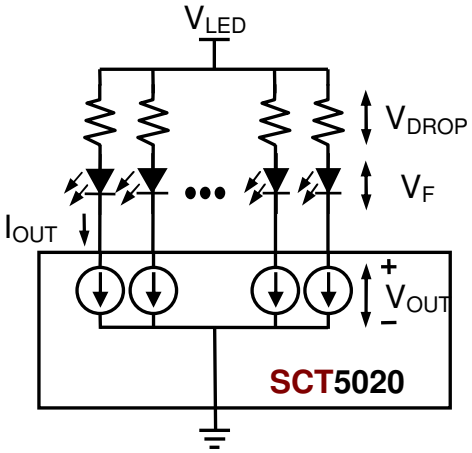
The output current can be kept constant when $V_{OUT} > V_{DO}$ (Drop out voltage). The relationship between I_{OUT} and V_{OUT} is as below. The output voltage should be kept as low as possible to prevent the SCT5020 from overheating.

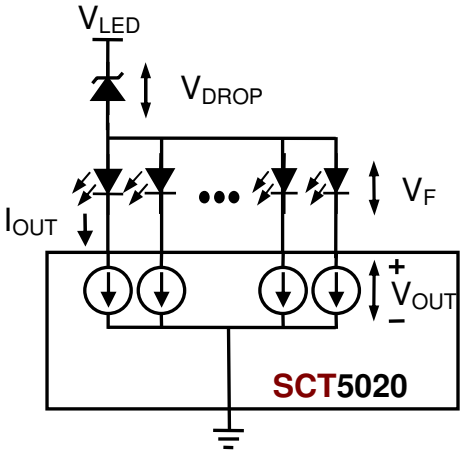




Load Supply Voltage (V_{LED})

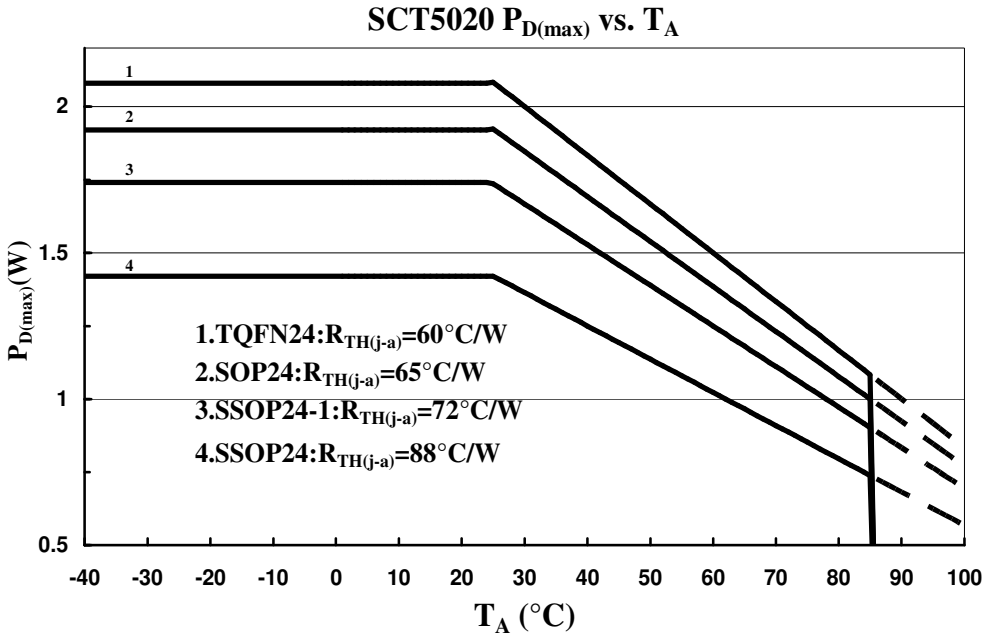
The SCT5020 works well when V_{OUT} is in the range of 1V to 4V. However, it is strongly recommended to use a voltage reducer to reduce the V_{OUT} voltage, which reduces the power dissipation of the SCT5020. We suggest that V_{OUT} is less than 1V. The voltage reducer can be a resistor or zener diode which makes $V_{OUT}=V_{LED}-V_{DROP}-V_F$.





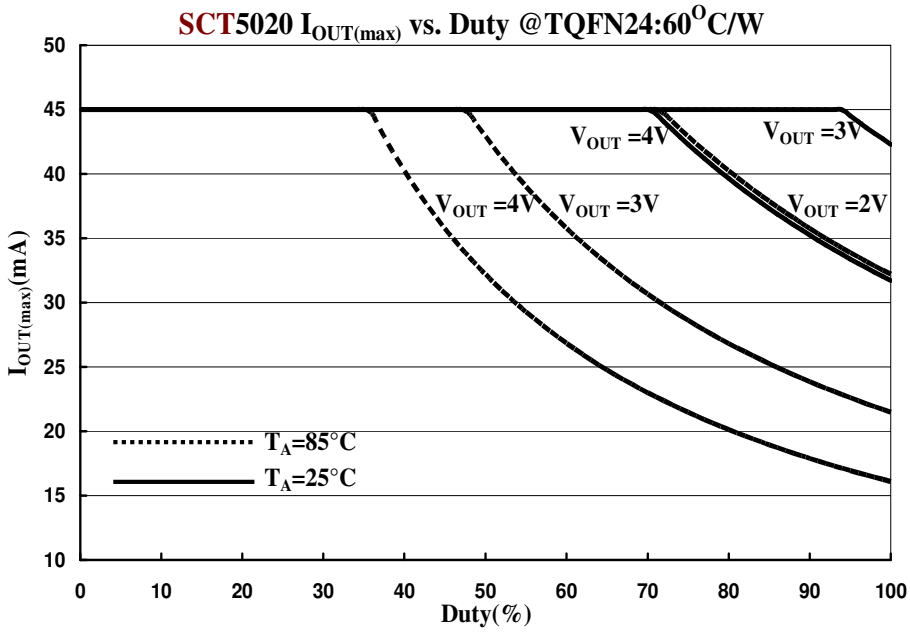
Power Dissipation

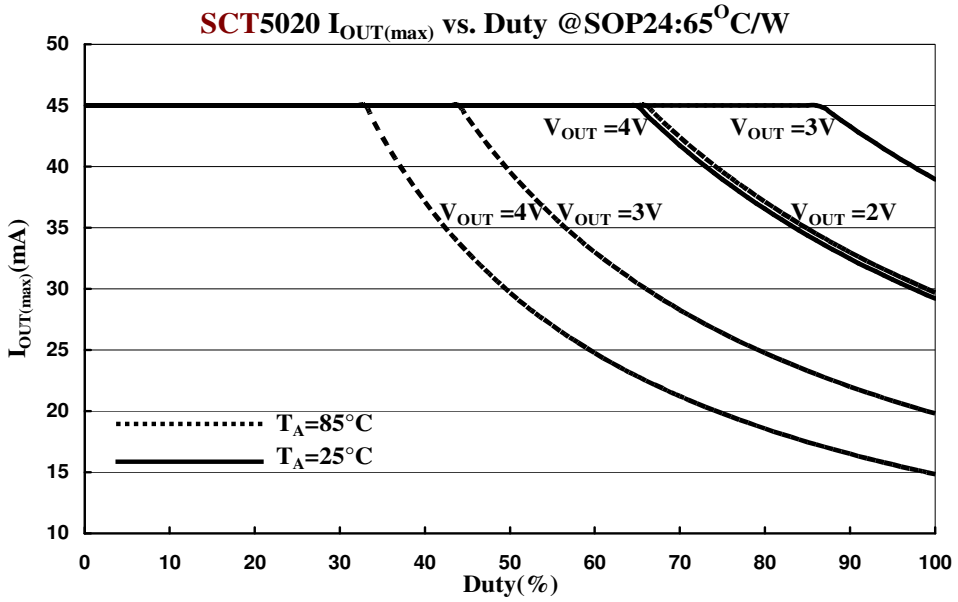
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with packages and ambient temperature. It is determined as $P_{D(max)}=(T_{J(max)} - T_A)/R_{TH(j-a)}$. Where $T_{J(max)}$ the maximum chip junction temperature is usually considered as 150℃, T_A the ambient temperature and $R_{TH(j-a)}$ thermal resistance. Since P(Watt)=IV, for sinking larger I_{OUT}, users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT5020.

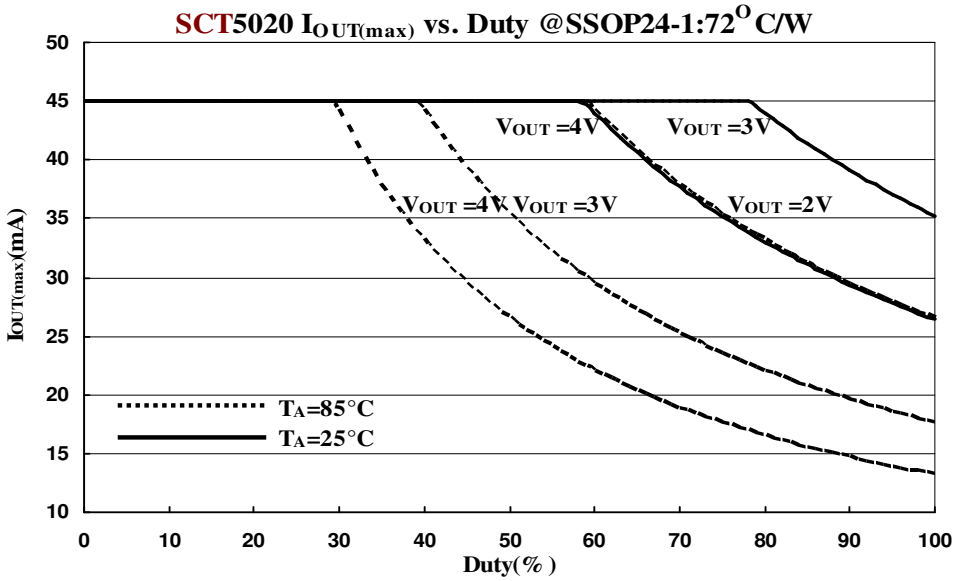


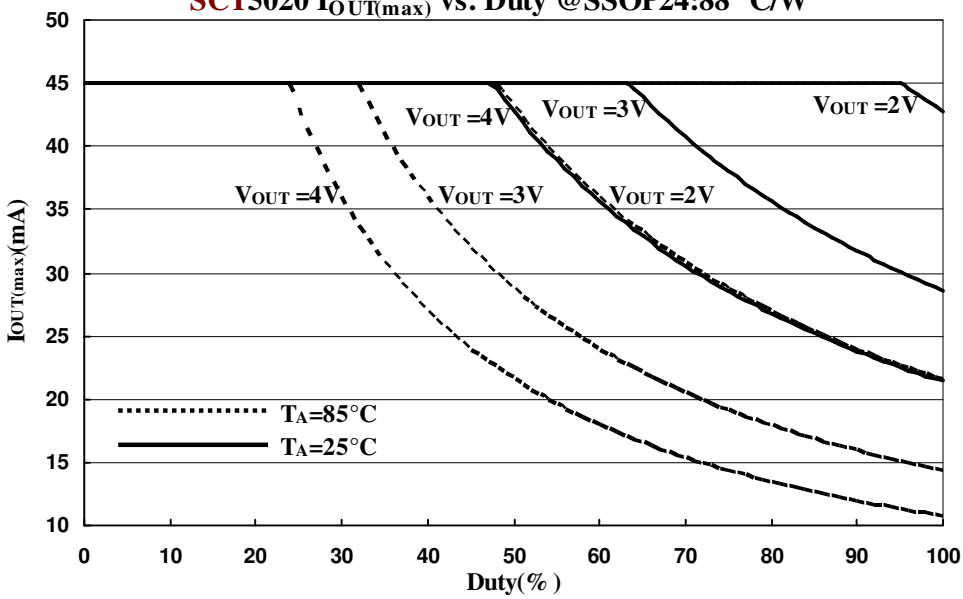
Limitation on Maximum Output Current

The maximum output current vs. output duty is estimated by:
$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-V_{DD}*I_{DD})/V_{OUT}/Duty/N$, where $T_{J(max)}$=150℃, N=16(all ON)

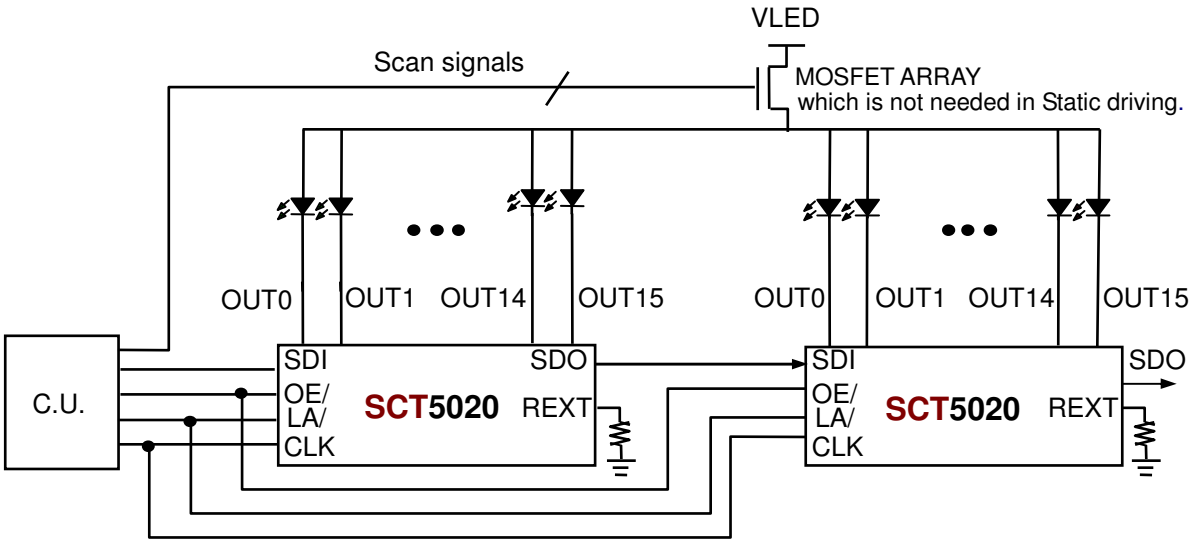



SCT5020 $I_{OUT(max)}$ vs. Duty @SOP24:65°C/W
$I_{OUT(max)}$(mA)
Duty(%)
VOUT =4V
VOUT =3V
VOUT =2V
VOUT =4V
VOUT =3V
TA=85°C
TA=25°C


SCT5020 $I_{OUT(max)}$ vs. Duty @SSOP24-1:72°C/W
IOUT(max)(mA)
Duty(%)
VOUT =4V
VOUT =3V
VOUT =2V
VOUT =4V
VOUT =3V
TA=85°C
TA=25°C


SCT5020 $I_{OUT(max)}$ vs. Duty @SSOP24:88°C/W
IOUT(max)(mA)
Duty(%)
VOUT =4V
VOUT =3V
VOUT =2V
VOUT =4V
VOUT =3V
VOUT =2V
TA=85°C
TA=25°C

Typical Application Circuits

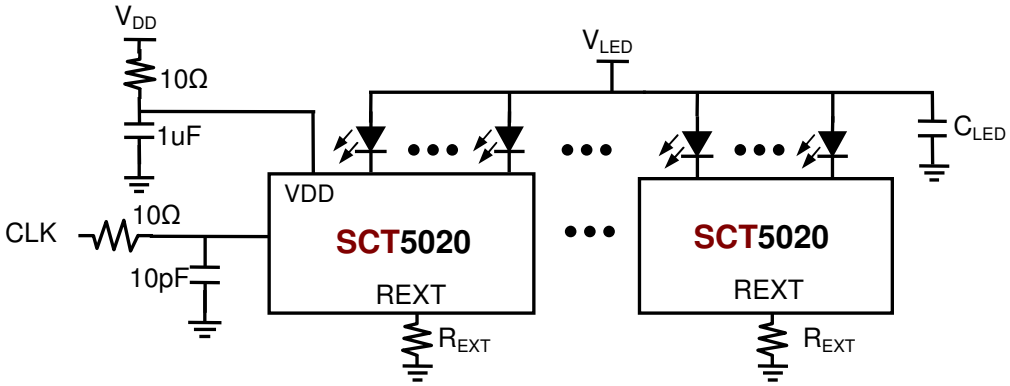


PCB Design Considerations

Use the following general guide-line when designing printed circuit boards **(**PCB**):**

Decoupling Capacitor

Place a 0.1uF or 1uF decoupling capacitor between VDD and GND pins of SCT5020. Locate the capacitor close to the SCT5020 as possible. A 0.1uF capacitor is normally adequate for static LED driving. But for dynamic scan or PWM applications, it is suggested to add capacitor of 1uF for each SCT5020. The required capacitance depends on the LED load current, the PWM switching frequency and the serial input data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies (VLED) can affect LED current regulation.



External Resistor (R_{EXT})

Locate the external resistor as close to the REXT pin as possible.

Power and Ground

Maximizing the width and minimizing the length of VDD and GND trace improve ground bouncing by effect of reducing parasitic resistance and inductance. A 10Ω resistor series in power input of the IC shunt with a 0.1uF decoupling capacitor is recommended. Separating power line V_{LED} for the LED and adding a 10uF capacitor C_{LED} beside the LED are also recommended.

EMI Reduction

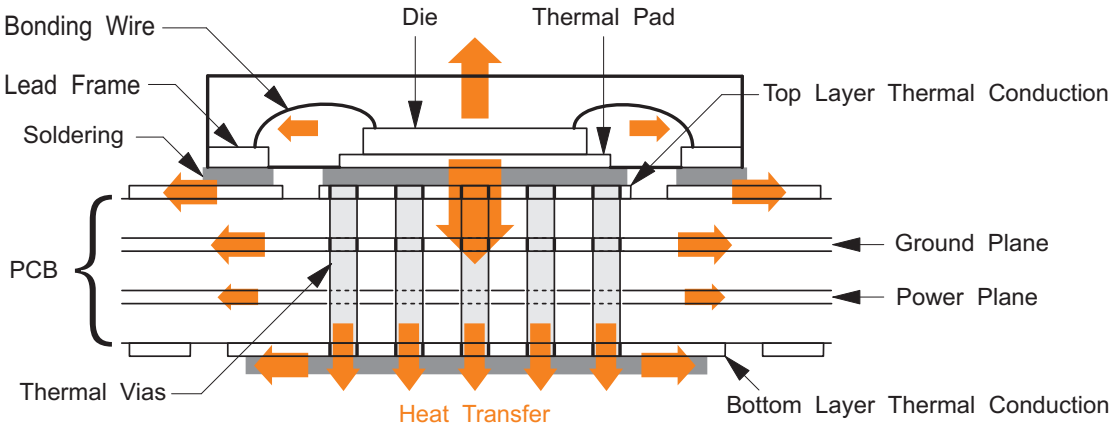
To reduce the EMI radiation from the system, an economical low pass filter (LPF) is recommended to slow down the transient edges of the clock signal. A four-layer PCB with two internal power and ground planes is a good scheme for shortening the signal path and reducing EMI radiation.

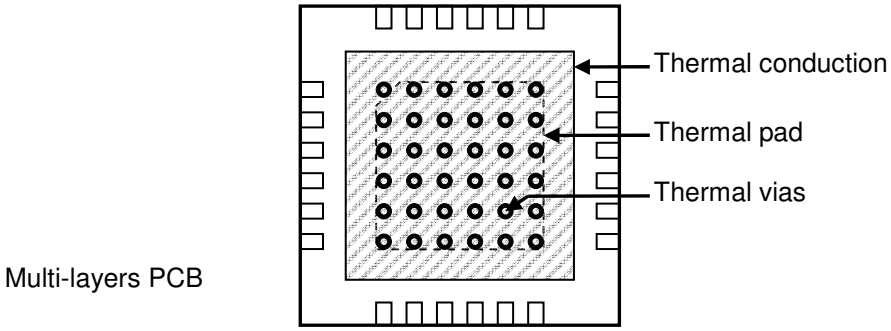
Thermal Pad Consideration

The “thermal pad” (or exposed pad) of TQFN package is used for heat dissipation. In most of applications, the thermal pad is electrically connected to ground plane to conduct heat directly.

To reduce thermal resistance, PCB designers should layout larger thermal conduction areas on top layer (component side) and bottom layer. In addition, the thermal via contact between the top layer and the bottom layer also needs to be as large as possible. Furthermore, increase the thickness of thermal conduction is an alternative.

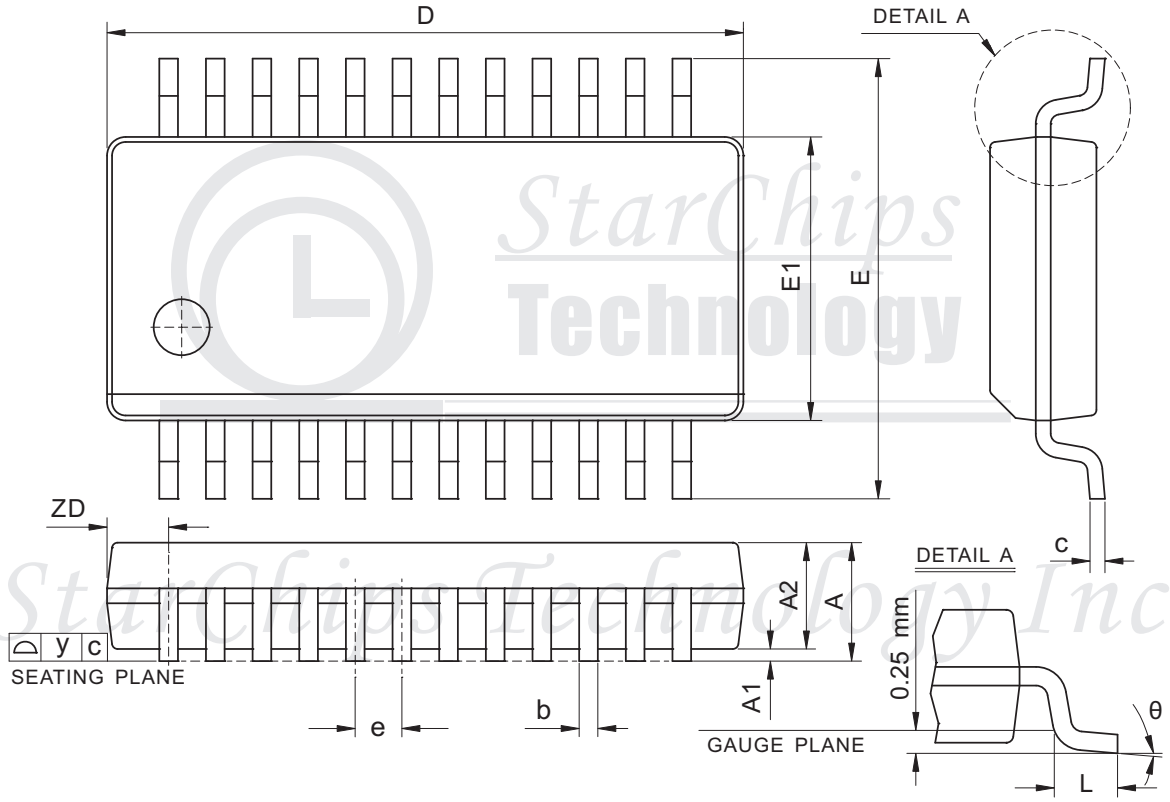
When making a solder paste screen, create an opening for the thermal pad. In this way, the thermal pad can be electrically and thermally connected to the PCB.





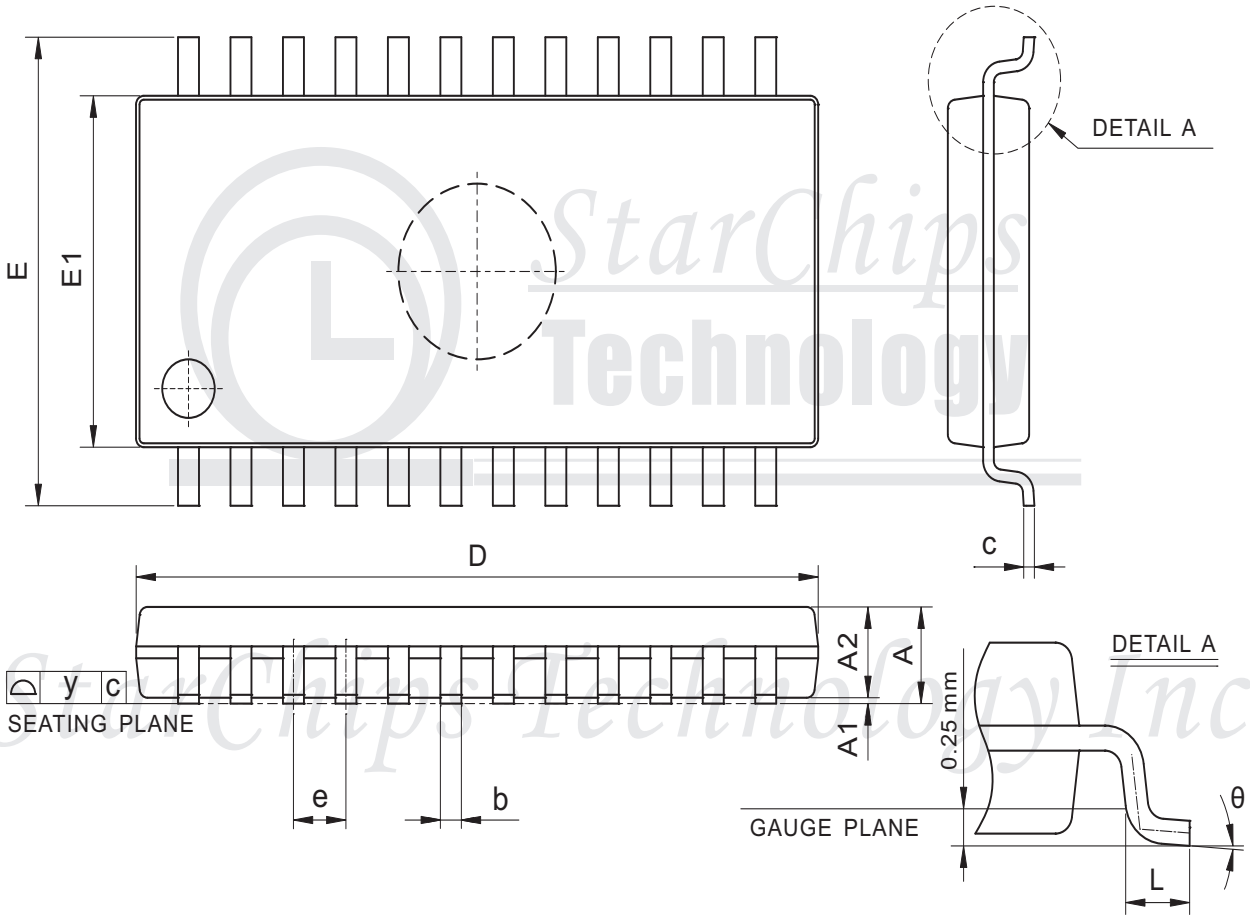
Package Dimension

SSOP24



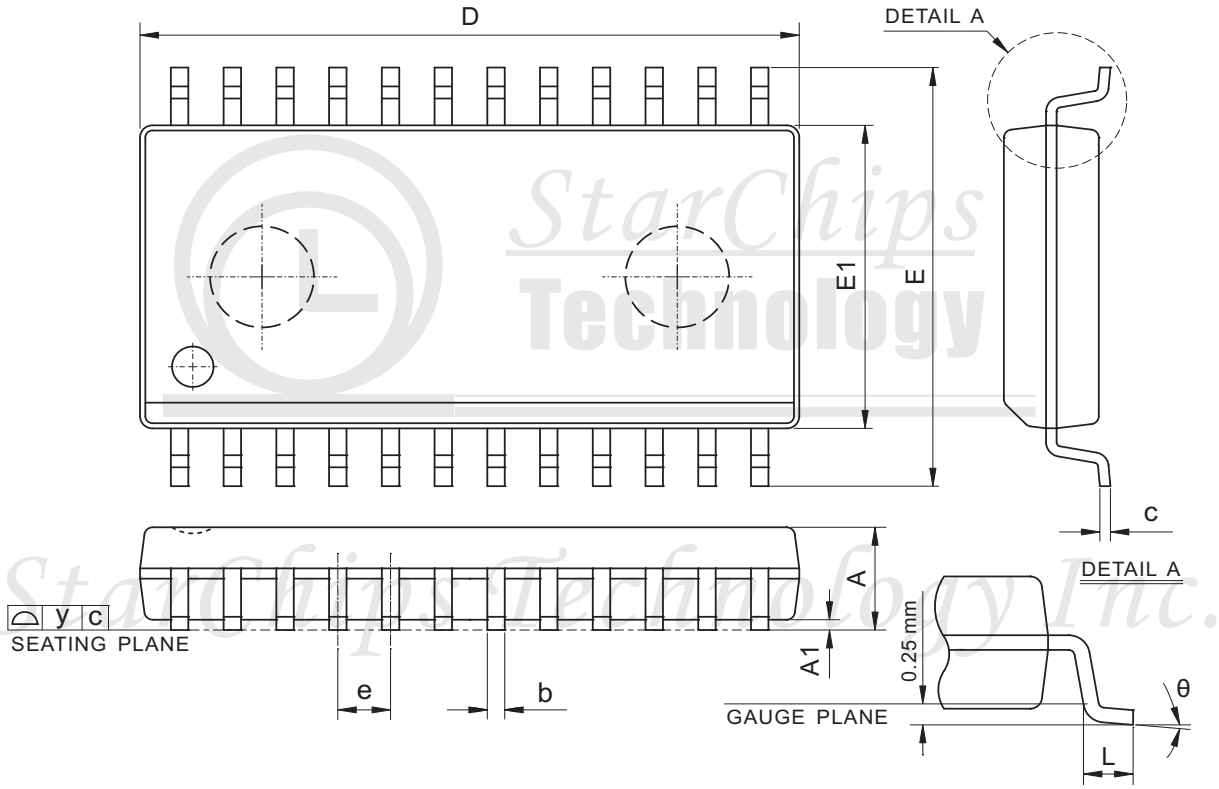
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.63	1.75	53.1	64.2	68.9
A1	0.10	0.15	0.25	3.9	5.9	9.8
A2	-	-	1.50	-	-	59.1
b	0.20	-	0.30	7.9	-	11.8
c	0.18	-	0.25	7.1	-	9.8
D	8.56	8.66	8.74	337.0	340.9	344.1
E	5.79	5.99	6.20	228.0	235.8	244.1
E1	3.81	3.91	3.99	150.0	153.9	157.1
e	0.64 BSC			25.0 BSC		
L	0.41	0.64	1.27	16.1	25.0	50.0
y	-	-	0.10	-	-	3.9
ZD	0.84 REF			33.0 REF		
θ	0°	-	8°	0°	-	8°

SSOP24-1



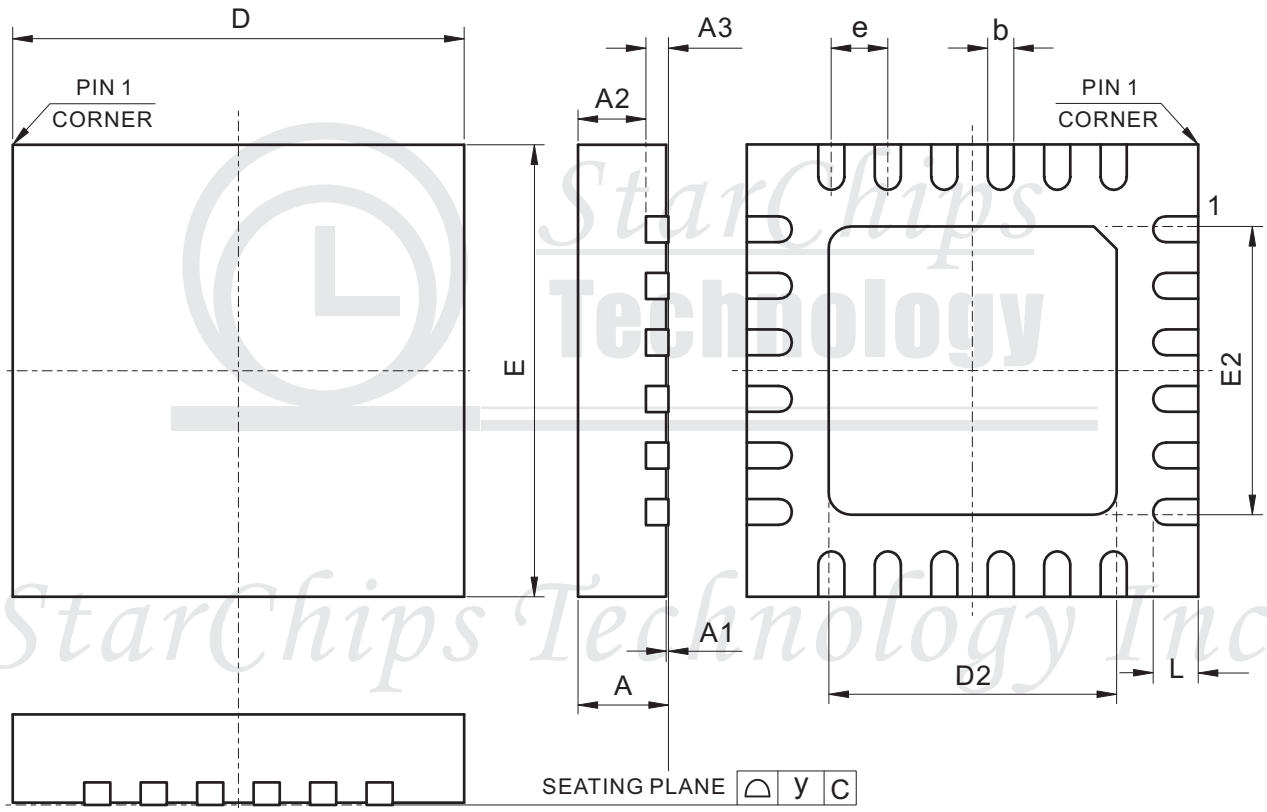
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.90	-	-	74.8
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.30	1.50	1.70	51.2	59.1	66.9
b	0.30	0.40	0.52	11.8	15.7	20.5
c	0.10	0.15	0.27	3.9	5.9	10.6
D	12.80	13.00	13.20	503.9	511.8	519.7
E	7.70	8.00	8.30	303.1	315.0	326.8
E1	5.80	6.00	6.20	228.3	236.2	244.1
e		1.00 BSC			39.4 BSC	
L	0.25	0.45	0.65	9.8	17.7	25.6
y	-	-	0.10	-	-	3.9
θ	0°	-	10°	0°	-	10°

SOP24



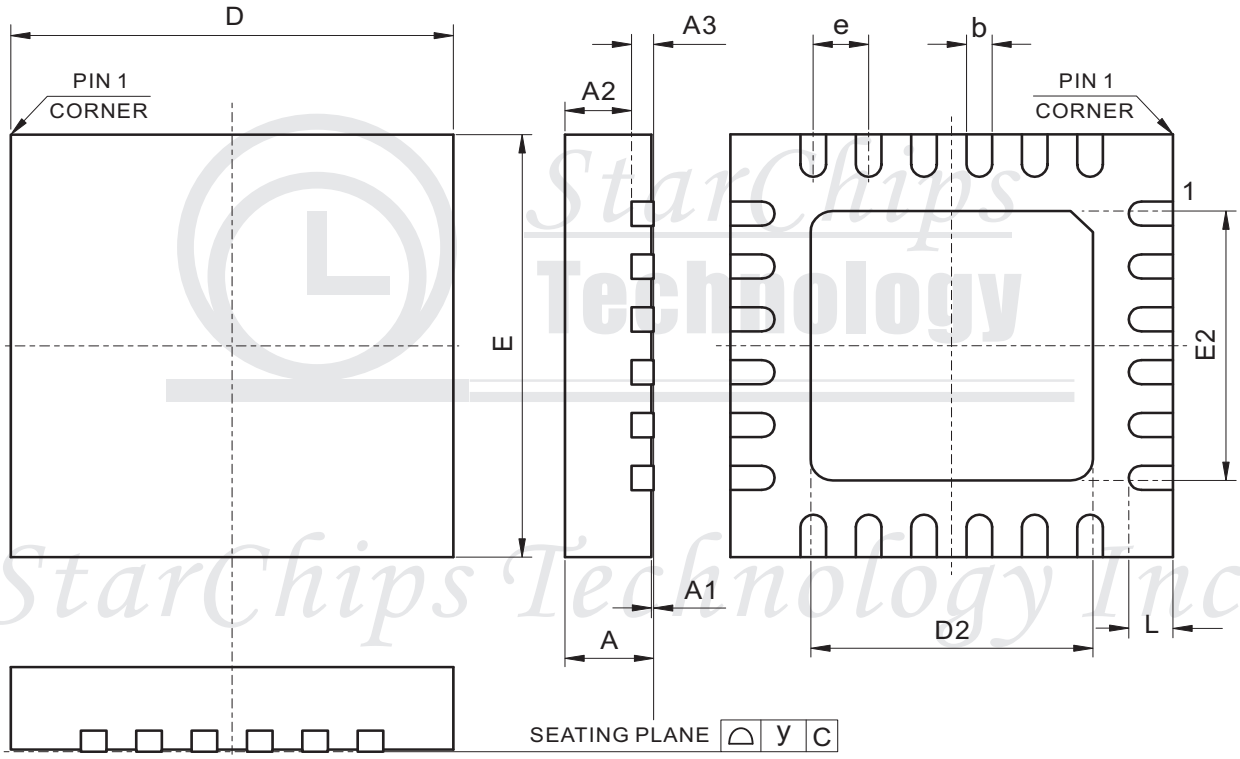
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.35	-	2.65	92.5	-	104.3
A1	0.10	-	0.30	3.9	-	11.8
b	0.33	-	0.51	13.0	-	20.1
c	0.23	-	0.32	9.1	-	12.6
D	15.20	-	15.60	598.4	-	614.2
E	10.00	-	10.65	393.7	-	419.3
E1	7.40	-	7.60	291.3	-	299.2
e	1.27 BSC			50.0 BSC		
L	0.40	-	1.27	15.7	-	50.0
θ	0°	-	8°	0°	-	8°
y	-	-	0.10	-	-	3.9

TQFN24-4x4(CQNG)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.76	0.80	0.84	30.0	31.0	33.0
A1	0.00	0.02	0.04	0.0	0.8	1.5
A2	0.57	0.60	0.63	22.0	24.0	25.0
A3		0.20 REF			8.0 REF	
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	154.0	157.0	161.0
D2	2.50	2.55	2.60	98.4	100.4	102.4
E	3.90	4.00	4.10	154.0	157.0	161.0
E2	2.50	2.55	2.60	98.4	100.4	102.4
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y	-	0.08	-	-	3.1	-

TQFN24-4x4(AQNG)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0.00	0.035	0.05	0.0	1.4	2.0
A2	-	0.55	0.57	-	21.7	22.4
A3	0.203 REF			8.0 REF		
b	0.20	0.25	0.30	7.9	9.8	11.8
D	4.00 BSC			157.0 BSC		
D2	2.40	2.50	2.60	94.5	98.4	102.4
E	4.00 BSC			157.0 BSC		
E2	2.40	2.50	2.60	94.5	98.4	102.4
e	0.50 BSC			19.7 BSC		
L	0.35	0.40	0.45	13.8	15.7	17.7
y	-	0.08	-	-	3.1	-

Revision History

Data Sheet Version	Remark
V01_01	First released
V02_01	ESD protection ability and IOUT updated

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